

316

(12) UK Patent Application (19) GB (11) 2 342 777 (13) A

(43) Date of A Publication 19.04.2000

(21) Application No 9924488.1

(22) Date of Filing 15.10.1999

(30) Priority Data

(31) 10294905 (32) 16.10.1998 (33) JP

(71) Applicant(s)

NEC Corporation
(Incorporated in Japan)
7-1 Shiba 5-chome, Minato-ku, Tokyo 108-01, Japan

(72) Inventor(s)

Kiyotaka Imai

(74) Agent and/or Address for Service

Mathys & Squire
100 Grays Inn Road, LONDON, WC1X 8AL,
United Kingdom

(51) INT CL⁷

H01L 27/088 21/8234

(52) UK CL (Edition R)

H1K KGAGX K1CA K11B4 K11D K11D1 K4C14 K9C2
K9D1

(56) Documents Cited

GB 2001197 A US 5495122 A US 4651406 A

(58) Field of Search

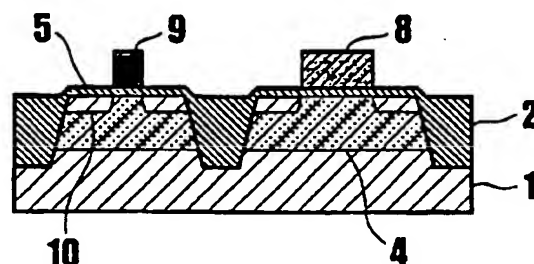
UK CL (Edition R) H1K KCAL KGAGX
INT CL⁷ H01L
ON LINE, W.P.I., EPODOC, JAP10

(54) Abstract Title

Gate electrodes for integrated mosfets

(57) A plurality of MOSFETs of one conductivity type having gate electrodes 8,9 formed of a semiconductor material are formed in a semiconductor substrate 1. The gate electrodes of these MOSFETs are implanted with an impurity at different concentrations in accordance with the threshold voltages to be set for the MOSFETs. Initially, an isolation region 2 and wells 4 are formed on the surface of the semiconductor substrate. Then a gate oxide film 5 is formed on the surfaces of the isolation region and the well. A polysilicon film for forming gate electrodes is then grown on the surfaces of the gate oxide film and the isolation region. A resist is then deposited to allow ion implantation in one gate region of the polysilicon film but prevent implantation in the other gate region. After removing the resist and patterning the polysilicon film to form first and second gate electrodes 8,9 a second impurity is implanted in the first and second gate electrodes and prospective source/drain regions 10.

FIG. 3F



GB 2 342 777 A